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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/059,644	04/13/1998	PAI-HUNG PAN	MI22-898	8771

21567 7590 05/20/2004

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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/059,644	PAN, PAI-HUNG	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *50,51 and 71-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *50,51 and 71-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's RCE and Amendment filed on February 23, 2004. Claims 1-49,52-70 were canceled. Claims 50-51,71-75 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claim 50 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Verhaar (5,015,598) in view of Park (5,545,578), with either Hiroki et al (5,512,771) or Kurimoto (5,306,655).

Verhaar teaches a method (at Figs 1-5; col 4, line 30 through col 5) for forming a conductive gate of a metal oxide transistor comprising the steps of: forming a gate oxide dielectric layer 11 on a substrate (col 4, lines 30-40); forming a conductive gate structure over the gate oxide dielectric layer 11, the gate structure comprising an insulative cap 13 (Figs 1-2; col 40-62) and having sidewalls defining a lateral dimension of the gate structure, the sidewalls comprising a polysilicon material surface 12 (col 4, lines 30-62); forming an oxidation preventing material 20 of silicon nitride as a non-oxide material 20 over the gate structure and the gate dielectric layer 11, the non-oxide material 20 being directly against the sidewalls along the entirety of the insulative cap 13 to and along the entirely of the polysilicon material surface 12 (Fig 3, col 4, line 63 through col 5, line3); anisotropically etching the non-oxide material 20 to form spacers 20a of silicon nitride on the sidewalls (Fig 4; col 5, lines 4-24), the spacers 20a laterally adjacent the gate structure and joining the gate dielectric layer 11 (Fig 4); exposing the substrate to oxidizing condition to channel oxidants through the gate dielectric layer 11 (col 5, lines 47-52) and underneath the spacers 20a joined with the gate dielectric layer 11 that is outwardly exposed laterally proximate the sidewall spacers, wherein only a bottom portion of the polysilicon gate electrode 12, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 11 is inherently oxidized (Fig 5), while the barrier insulating nitride spacers 20a prevents oxidation of the upper parts of side faces of the polysilicon gate electrode 12 (col 5, lines 35-61). Since Verhaar discloses oxidizing at 900°C for a duration of 15 to 30 minutes in oxygen to form a silicon oxide layer 24 (fig 5) having a thickness of the order of 10 to 15 nm (100 to 150 Angstroms), wherein the silicon nitride spacers 20a has a thickness between

15 and 50 nm and preferably close to 30 nm (col 4, lines 63-68) adjacent to the gate electrode 12, only a portion only a portion of the gate electrode 12, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10 is inherently oxidized and creating a "smiling gate" (can be seen by enlarging the polysilicon gate electrode 12), wherein as shown from Figures 4 to 6 of Verhaar, after forming spacers 20a and prior to forming source and drain regions 22a,23a (Fig 6), exposing the substrate to oxidizing conditions to create a "smiling gate" (Figs 4-6). It is the fact that the present specification discloses (at page 7, lines 14-19) that only portion of the gate electrode is oxidized in a time period for growing "an oxide layer over a separate semiconductor substrate to a thickness of a round 80 Angstroms". Herein, since Verhaar grows a silicon oxide layer 24 having a thicker thickness of 100 to 150 Angstroms, only a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10, is inherently oxidized ("smiling gate"). Consequently, the burden shifted to applicant to demonstrate and prove that this apparent inherence does not in fact exist, In re King, 801 F.2d 1324, 1327, 231 USPQ 136, 138-139 (Fed. Cir. 1986).

Re claim 50, Verhaar already forms the gate structure having sidewalls comprising a layer 12 for a polysilicon material surface, but mainly lacks including a metal-comprising surface layer on the polysilicon layer.

However, Park et al teach (; and Fig 4, col 4, line 25 through col 5; and Fig 1 col 1, lines 11-65) forming a gate structure having sidewalls, the sidewalls comprising a layer 14a for a polysilicon material surface (Fig 4G), an overlying metal layer 16a for a metal-comprising surface formed over the polysilicon layer 14a, and a top nitride cap layer 18a thereon, wherein nitride sidewall spacers 22a are formed on sidewalls of the gate structure and along the entirety of the metal-comprising surface layer 16a, wherein a only portion of the polysilicon layer 14a of the gate structure is oxidized (col 5, lines 3-14; Fig 1F).

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the gate structure comprising an insulative cap 13 and the polysilicon material layer 12 of Verhaar by forming a metal-comprising surface of tungsten on the polysilicon material surface layer 12, between the insulative cap 13 and the polysilicon layer 12a, as taught by Park. This is because of the desirability to increase electrical conductivity

of the gate structure since the metal has lower resistance than polysilicon, and because of the desirability to fabricate devices having high operational speed.

Moreover, regarding of forming a "smiling gate" by oxidizing a corner bottom portion of the gate electrode. As under 103 rejection and as evidence: *Hiroki et al* '771 teach forming a "smiling gate" by oxidizing a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, wherein the oxide layer 6' underlying the silicon nitride spacer 7 allows oxidizing substance to transmit therethrough to oxidize a portion of the gate electrode of polysilicon material to form a "smiling gate" (col 12, lines 10-21; figs 6A-6B), wherein as shown from Figure 6A to Figure 6D of Hiroki, after forming spacers and prior to forming source and drain regions 3 (Fig 6D; col 12), the gate structure is exposed to oxidizing conditions to create a "smiling gate" (Figs 6B-6C), wherein the spacers protect at least a portion of the polysilicon material of the gate electrode. *Kurimoto* teaches (at Figs 13a-13h; col 13, line 21 through col 16) forming a gate structure having a gate electrode 5f on a gate oxide dielectric layer 2 (figs 13a; col 13, lines 30+); forming barrier sidewall nitride spacers 10 over sidewalls of the gate electrode and joining the dielectric oxide layer 2 by anisotropically etching a silicon nitride layer 10 (figs 13C-13D); and then oxidizing by channeling oxidants through the dielectric layer, wherein only a portion of the gate electrode 5f, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 2 is oxidized during this oxidation due to the existence of nitride sidewall spacer 10 (col 13, lines 59-68) and insulating cap layer 9, wherein oxidants channels through the gate dielectric layer 2 and underneath the spacers joined therewith. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to create a "smiling gate" as taught by Hiroki and Kurimoto by oxidizing a portion of the gate electrode of Verhaar, wherein a portion of the oxide layer 11 underlying the spacers 20a as shown in figure 11 allows oxidizing substance to transmit therethrough to oxidize a portion of the gate electrode to form a "smiling gate". This is because of the desirability to have smaller gate-to-drain capacitance and thus to improve the speed of the circuit operation (col 8, lines 45-67; fig 2).

2. Claim 75 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Verhaar (5,015,598) in view of Park (5,545,578), with Hiroki et al (5,512,771) or Kurimoto (5,306,655), as applied to claim 50, and further of Pierce (5,422,289) and Iijima et al (5,903,053).

The references including Verhaar and Park teach a method for forming a transistor gate as applied to claim 50 above. Re further claim 75, Park also teaches forming the metal-comprising surface layer of tungsten silicide 16/16a on the polysilicon layer 14 (Fig 4; col 4, lines 25-50).

Re claim 75, the references thus lack listing at least one of W, Mo, TiN, and WN for the metal-comprising surface.

However, Pierce teaches (at col 9, lines 35-50; Figs 1-5) forming a gate structure including a metal-comprising surface layer 28 formed on a polysilicon material surface layer 20, wherein the metal-comprising surface layer 28 includes refractory metal silicide, tungsten (W), titanium nitride (TiN), molybdenum (Mo), etc. Iijima teaches (at Fig 19, col 21, lines 30-63; and Fig 21, col 23, line 57 through col 24, line 65) forming a gate structure including a metal-comprising surface layer (308 in Fig 19E; 508 in Figs 21E-21K) formed on a polysilicon material surface layer 207/507, wherein the metal-comprising surface layer includes refractory metal silicide, tungsten nitride (WN).

Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate structure of the combined references including Verhaar and Park by alternatively employing at least one of W, Mo, TiN, and WN for the metal-comprising surface on the polysilicon layer, as further taught by Pierce and Iijima. This is because of the desirability to lower resistance of the gate structure so as to improve operational speed of the device, wherein W, Mo, TiN, and WN are art recognized equivalent metals for substitution, and are metal material having high electrical conductivity.

3. Claims 51,71-74 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Verhaar (5,015,598) and Park '578, with either Hiroki '771 or Kurimoto '655, as applied above to claim 50, and further of Kumagai (5,430,313) and Brigham (5,714,413).

The references including Verhaar and Park teach a method for forming a transistor gate as applied to claim 50 above. The references including Verhaar and Kurimoto already teaches

forming single sidewall barrier spacers over sidewalls of the gate (similarly to a first embodiment of the present invention as shown in figure 3 having a single sidewall barrier spacers 34). Moreover, Verhaar also discloses (at col 4, line 63 through col 5, line 24; Fig 4) forming the silicon nitride spacers 20a by depositing the non-oxide material 20 of silicon nitride having a thickness lying between 15 and 50 nm (150-500 Angstroms). Park also teach (at col 4, lines 52-65; Figs 4D-4E) depositing the non-oxide material 22 of silicon nitride having a thickness lying between 50-500 Angstroms, and anisotropically etching to form the silicon nitride spacers 22a.

The further difference between the references applied above and the instant claim(s) are as follows: either using single sidewall spacers (as in claim 50, first embodiment shown in Fig 3 of present application), using double sidewall spacers by anisotropically etching twice (as in claims 51,71,72, second embodiment shown in Fig 5), or using double sidewall spacers by anisotropically etching first and second material layers (as in claims 73-74, third embodiment shown in Fig 7).

However, re claims 51,71-72, Kumagai teaches (at figs 4B-4D; col 3, line 65 through col 4, line 15) forming single sidewall nitride spacers 16 on sidewalls of a gate 14, and alternatively, forming double sidewall nitride spacers including first sidewall nitride spacers 16 and second sidewall nitride spacers 30 by anisotropically etching a deposited first material barrier layer and then anisotropically etching a second deposited material barrier layer (figs 7A-7D; col 5, line 45 through col 6), wherein, re claim 73, prior to anisotropically etching the non-oxide material of nitride 48 (col 7, lines 39-43; Fig 10-11D), and anisotropically etching the nitride layer 16. Brigham teaches (at figs 2b-2c,3c; col 6, line 60 through col 7, line 6; cols 4-6) forming double sidewall spacers by depositing a second material layer on a first material layer and anisotropically etching both the first and second layers to form double sidewall spacers, wherein Brigham expressly teaches "three or more layers of dielectric...are implemented to form a multi-layered spacer structures" (col 7, lines 1-6), and wherein silicon nitride is disclosed.

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to form the spacers of Verhaar by alternatively forming single sidewall nitride spacers or double sidewall spacers on the sidewalls of the gate as combinatively taught by Kumagai and Brigham, and Verhaar. This is because of the desirability to substitute and alternatively use the single sidewall nitride spacers or the double sidewall spacers as a barrier

mask during oxidation to form an oxide film. This is also because of the desirability to employ the double sidewall spacers as a mask during implantation to form source and drain regions at a predetermined distance from the gate electrode.

Furthermore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to form the non-oxide material of nitride by selecting the portion of the prior art's range of thickness between 150-500 Angstroms, as taught by Verhaar, and of a thickness between 50-500 Angstroms, as taught by Park et al, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation, see In re Aller, etal., 105 USPQ 233; In re Waite 77 USPQ 586 (CCPA 1948); In Re Swanson 56 USPQ 372 (CCPA 1942).

Response to Arguments

4. Applicant's remarks filed February 23, 2004 have been fully considered but they are not persuasive, and are moot in view of new ground(s) of rejection.

Applicant mainly remarked that "...Verhaar does not disclose or suggest the recited gate structure having sidewalls comprising a polysilicon material surface and a metal-comprising surface...forming a non-oxide material directly against the sidewalls along an entirety of the polysilicon material surface and along an entirety of the metal-comprising surface...".

In response, this is noted and found unconvincing. This is a 35 USC 103 rejection. Herein, Park prima facie teaches forming the gate structure by forming a metal-comprising surface layer 16a on a polysilicon gate 14a, with a top nitride insulating cap 18a formed on the metal-comprising surface layer 16a, wherein nitride sidewall spacers 22a are formed on sidewalls of the gate structure and along the entirety of the metal-comprising surface layer 16a, wherein a only portion of the polysilicon layer 14a of the gate structure is oxidized (col 5, lines 3-14; Fig 1F). Herein Verhaar, as a main references, teaches forming a non-oxide material of nitride spacers 20/20a against the sidewalls and along the entirety of the sidewalls including the polysilicon surface layer 12 and the insulative cap 13. Thus, in combining of the references, by forming the metal-comprising surface layer on the polysilicon layer 12 of Verhaar, between the

insulative cap 13 and the polysilicon layer 12, the subsequently deposited non-oxide material of nitride spacers 20/20a are consequently formed directly against the sidewalls and along the entirety of the sidewalls including the insulative cap 13, the newly added metal layer, and polysilicon layer 12. Accordingly, the rejection is not overcome by pointing out that one reference does not contain a particular limitation when reliance for that teaching is on another reference. In Re Lyons 150 USPQ 741 (CCPA 1966). Applicant has argued and discussed the references individually without clearly addressing the combined teachings. It must be remembered that the references are relied upon in combination and are not meant to be considered separately as in a vacuum. It is the combination of all of the cited and relied upon references which make up the state of art with regard to the claimed invention. Applicant's claimed invention fails to patentably distinguish over the state of the art represented by the cited reference. It is well settled that one can not show non-obviousness by attacking the references individually where, as here, the rejection is based on combinations of references. In re Young, 403 F.2d 754,159 USPQ 725 (CCPA 1968); In re Keller 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Indeed, as evidently shown in Figure 5 of Pierce (5422,289), the non-oxide sidewall spacers 32 is formed directly against the sidewalls along the entirety of the polysilicon material surface layer 10 and along the entirety of the metal-comprising surface layer 28. Also, as shown in Figure 21I-21J of Iijima (5,903,053), the non-oxide material of nitride spacers 515/516 is formed against the sidewalls along the entirety of the polysilicon material surface layer 507 and along the entirety of the metal-comprising surface layer 508/509. Accordingly, the rejections are outstanding.

Kumagai and Brigham are cited to show the formation of the single spacer, L-shaped double sidewall spacers by etching first and second material layers, and double sidewall spacers by depositing and anisotropically etching the first material layer and then depositing and anisotropically etching a second material layer. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Verhaar to alternatively form single sidewall nitride spacers or double sidewall spacers on the sidewalls of the gate as taught by Brigham, Kumagai, and Verhaar. This is because of the desirability to substitute and alternatively use the single sidewall nitride spacers or the double sidewall spacers as a barrier

mask during oxidation to form an oxide film. This is also because of the desirability to employ the double sidewall spacers as a mask during implantation to form source and drain regions at a predetermined distance from the gate electrode. The rejection is not overcome by pointing out that one reference does not contain a particular limitation when reliance for that teaching is on another reference. In Re Lyons 150 USPQ 741 (CCPA 1966). It is well settled that one can not show non-obviousness by attacking the references individually where, as here, the rejection is based on combinations of references. In re Young, 403 F.2d 754,159 USPQ 725 (CCPA 1968); In re Keller 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-01

Michael Trinh
Primary Examiner